WHAT IS CLAIMED IS:

1. A data processing apparatus comprising at least a first information processing device and a signal line connected to said information processing device, said data processing apparatus having a means for changing power consumption on said signal line during transmission of a signal through said signal line in accordance with an actual state of said power consumption that would be observed when said means were not used.

2. A data processing apparatus comprising at least a first information processing device and a second information processing device connected to said first information processing device by a signal line, said data processing apparatus determining a state of second power consumption for a state of first power consumption on said signal line during transmission of a signal through said signal line from at least one of said first information processing device and said second information processing device in such a way that said second power consumption is distributed over a period to complement said first power consumption.

3. An information processing device having at least a signal line connected to said information processing device wherein said information processing device

claims 1-6, 13-19, 24, 25
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determines a state of second power consumption for a state of first power consumption on said signal line during transmission of a signal of said information processing device through said signal line in such a way that a sum of said second power consumption and said first power consumption is equal to a desired value.

4. An information processing device having at least a signal line connected to said information processing device wherein said information processing device determines a state of second power consumption for a state of first power consumption on said signal line during transmission of a signal of said information processing device through said signal line in such a way that, in a period said first power consumption exists, said second power consumption is not generated but, in a period said first power consumption does not exist, said second power consumption is generated.

5. An information processing device having at least a signal line connected to said information processing device wherein power consumption is generated for an inverted value of a digital signal of said information processing device transmitted through said signal line.

6. A data processing apparatus comprising at least a first information processing device and a second information processing device connected to said first

information processing device by a signal line, said data processing apparatus having a means for determining a state of second power consumption for a state of first power consumption on said signal line during transmission of a digital signal through said signal line from at least one of said first information processing device and said second information processing device in such a way that said second power consumption is power consumption generated for an inverted value of a digital signal of said information processing device transmitted through said signal line.

7. An information processing device having at least a signal line connected to said information processing device wherein, between said information processing device and said signal line, a signal from said information processing device can be encrypted and an encrypted signal transmitted from said signal line can be decrypted.

8. A data processing apparatus comprising at least a first information processing device and a second information processing device connected to said first information processing device by a signal line wherein, between at least either said first information processing device or said second information processing device and said signal line, a signal from said first information processing device or said second information processing device can be encrypted and a signal transmitted from said

signal line can be decrypted.

9. A data processing apparatus comprising at least a first information processing device and a second information processing device connected to said first information processing device by a signal line wherein:

a signal from said first information processing device is encrypted and said encrypted signal from said first information processing device is decrypted before being supplied to said second information processing device; and

a signal from said second information processing device is encrypted and said encrypted signal from said second information processing device is decrypted before being supplied to said first information processing device.

10. A data processing apparatus comprising at least an information processing device, an information memory device and a signal line connected at least to said information processing device wherein:

at least in an operation to store information into said information memory device, said information is encrypted; and

information stored in said information memory device can be decrypted.

11. A data processing apparatus comprising at least an information processing device, an information memory

device and a signal line connected at least to said information processing device wherein:

at least in an operation to store information into said information memory device, said information is encrypted; and

information stored in said information memory device can be decrypted before supplying said information through said signal line to said information processing device.

12. An information processing device having at least a signal line connected to said information processing device wherein an original order of a signal series output by said information processing device can be changed to another order prior to transmission through said signal line and said other order can be restored back to said original order.

13. A data processing apparatus comprising at least a first information processing device, a second information processing device, a signal line connecting said first information processing device to said second information processing device, a control-signal generation means and a means for consuming a second power different from a first power consumed by said signal line wherein:

said first or second information processing device is connected to said means for consuming said second power;

a control signal generated by said control-signal

generation means is used for execution of a control technique not to clear a signal asserted on said signal line; and

in a transfer of a present signal between said first and second information processing devices through said signal line, an exclusive logical OR of said present signal output by said first or second information processing device, a previous signal asserted on said signal line immediately before and a signal supplied to a charging & discharging device employed in said means for consuming said second power immediately before is computed, and said sum is supplied to said charging & discharging device in accordance with another control signal generated by said control-signal generation means so that a sum of said first power and said second power is equal to a predetermined value.

14. A data processing apparatus comprising at least a first information processing device, a second information processing device, a signal line connecting said first information processing device to said second information processing device, a control-signal generation means and first and second means each for consuming a second power different from a first power consumed by said signal line wherein:

said first information processing device is

connected to said first means for consuming said second power whereas said second information processing device is connected to said second means for consuming said second power;

a control signal generated by said control-signal generation means is used for execution of a control technique not to clear a signal asserted on said signal line; and

in a transfer of a present signal between said first and second information processing devices through said signal line, an exclusive logical OR of said present signal output by said first or second information processing device, a previous signal asserted on said signal line immediately before and a signal supplied to a charging & discharging device employed in said first or second means for consuming said second power immediately before is computed, and said sum is supplied to said charging & discharging device in accordance with another control signal generated by said control-signal generation means so that a sum of said first power and said second power is equal to a predetermined value.

15 A data processing apparatus according to claim 13, wherein said second means for consuming said second power has a dummy signal line.

16. A data processing apparatus according to claim

14 wherein said second means for consuming said second power has a dummy signal line.

17. A data processing apparatus comprising at least a first information processing device, a second information processing device, a signal line connecting said first information processing device to said second information processing device, a precharge-signal control means and a means for consuming a second power different from a first power consumed by said signal line wherein:

said first or second information processing device is connected to said means for consuming said second power;

said second or first information processing device is connected to said precharge-signal control means; and

in a transfer of a signal between said first and second information processing devices through said signal line, a sum of a consumption amount of said first power and a consumption amount of said second power is controlled to become equal to a predetermined value.

18. A data processing apparatus comprising at least a first information processing device, a second information processing device, a signal line connecting said first information processing device to said second information processing device and a signal line precharge control device for precharging said signal line wherein:

said first information processing device is

connected to said signal line precharge control device and a compensatory precharge bus control device;

said compensatory precharge bus control device is connected to said signal line;

said compensatory precharge bus control device is connected to a means for consuming a second power different from a first power consumed by said signal line; and

bits of data flowing through a bus is inverted immediately after precharging said signal line before being supplied to said means for consuming said second power so that a sum of a consumption amount of said first power on said data signal line and a consumption amount of said second power becomes equal to a predetermined value.

19. A data processing apparatus according to claim 17 wherein said second means for consuming said second power has a dummy signal line.

20. A data processing apparatus comprising at least a first information processing device, a second information processing device, a signal line connecting said first information processing device to said second information processing device and a signal line precharge control device for precharging said signal line wherein:

said signal line has an inversion device in the middle of said signal line; and

said signal line on one side of said inversion

device is a signal line of positive logic while said signal line on the other side of said inversion device is a signal line of negative logic.

21. A data processing apparatus comprising at least an information processing device, an information memory device and a signal line connecting said information processing device to said information memory device wherein:

encryption can be carried out between said information processing device and said signal line; and

decryption can be carried out between said signal line and said information memory device.

22. An information memory device for storing a plurality of pieces of information at the same plurality of storage locations wherein:

said information memory device is divided by address into said plurality of said storage locations;

information can be written into and read out from each of said storage locations;

information to be recorded into any of said storage locations is encrypted; and

information read out from any of said storage locations is decrypted.

23. A data processing apparatus comprising at least an external information memory device, an information

processing device including an internal information memory device, a signal line connecting said external information memory device to said information processing device and an information-transfer control device for controlling a transfer of information between said external information memory device and said information processing device wherein said information-transfer control device comprises:

a source address register for storing an address in a transfer source at which information to be transferred is stored;

a destination address register for storing an address in a transfer destination at which said information to be transferred will be stored;

a counter for storing a value for counting the number of pieces of information to be transferred;

a counter processing circuit for decrementing said value stored in said counter;

a data buffer for temporarily storing information being transferred between said external information memory device and said internal information memory device;

a register processing circuit for updating said address stored in said source address register and said address stored in said destination address register;

a randomization circuit for randomizing a transfer order of said address stored in said source address

register and said address stored in said destination address register;

an address buffer for temporarily storing an address obtained as a result of randomization carried out by said randomization circuit; and

a control circuit for controlling said source address register, said destination address register, said counter, said counter processing circuit, said register processing circuit, said randomization circuit, said data buffer and said address buffer.

24. A card comprising at least a first information processing device and a second information processing device connected to said first information processing device by a signal line, said data processing apparatus having a means for changing power consumption on said signal line during transmission of a signal through said signal line in accordance with an actual state of said power consumption that would be observed when said means were not used.

25. An information processing system comprising at least a terminal and a card connectable to said terminal wherein said card comprises at least a first information processing device and a second information processing device connected to said first information processing device by a signal line, and there is provided a means for

changing power consumption on said signal line during transmission of a signal through said signal line in accordance with an actual state of said power consumption that would be observed when said means were not used.